Listing of the Claims

1.-3. (Canceled).

4. (Previously Presented) An array substrate comprising:

a first gate line;

a second gate line that is electrically insulated from the first gate line;

a data line crossing the first and second gate lines to define a pixel region that includes first and second regions;

a first switching device that is electrically connected to the first gate line and the data line;

a second switching device that is electrically connected to the second gate line;

a transmissive electrode that is electrically connected to the second switching device, the transmissive electrode being formed in the first region;

a reflective electrode that is electrically insulated from the transmissive electrode, the reflective electrode being formed in the second region that is adjacent to the first region; and

a compensating wiring that is electrically connected to the first switching device, the same compensating wiring facing the reflective electrode and the transmissive electrode with an insulation layer interposed between the compensating wiring and the reflective electrode and between the compensating wiring and the transmissive electrode.

5. (Original) The array substrate of claim 4, wherein the first switching device corresponds to a first thin film transistor including a gate electrode that is electrically

connected to the second gate line, a source electrode that is electrically connected to the data line, and a drain electrode that is electrically connected to the compensating wiring.

6. (Original) The array substrate of claim 4, wherein the second switching device corresponds to a second thin film transistor including a gate electrode that is electrically connected to the first gate line, a source electrode that is electrically connected to a ground voltage, and a drain electrode that is electrically connected to the transmissive electrode.

7. (Original) The array substrate of claim 6, further comprising a third thin film transistor that includes a gate electrode that is electrically connected to the first gate line, a source electrode that is electrically connected to the data line, and a drain electrode that is electrically connected to the compensating wiring.

8. (Original) The array substrate of claim 4, wherein the second switching device corresponds to the second thin film transistor including a gate electrode that is electrically connected to the first gate line, a source electrode that is electrically connected to the data line, and a drain electrode that is electrically connected to the transmissive electrode and the compensating wiring.

9. (Original) The array substrate of claim 4, further comprising a circuit for allowing the first gate line to maintain a first driving signal until the second gate line receives a second driving signal.

10. (Original) The array substrate of claim 4, wherein the compensating wiring and the data line are formed from a same layer.

11. – 29. (Cancelled).